Amendments to the Claims

1. (Currently amended) A content addressable arrayed control system, comprising a plurality of control cells each comprising a plurality of memory cells, each memory cell receiving a respective one of a plurality of data lines distributed to all of said control cells and a respective one of a plurality of timing lines distributed to all of said control cells, and a load line distributed only to one of the control cells of said plurality of control cells, each memory cell comprising:

a 1-bit latch triggered by said load line to latch a signal on said respective data line; and

a 1-bit comparator comparing an output of said latching circuit with a signal on said respective timing line and outputting a valid bit compare signal on an output line commonly connected to the comparators of all memory [[cell]] <u>cells</u> of said control cell, an address compare signal on said output line being valid only when all of said comparators of said control cell output valid bit compare signals.

2. (Currently amended) The system of Claim 1, wherein each control cell further includes an output latch latching in response to said output signal a state signal on a state line distributed to all output latches of [[said]] said plurality of control cells.

3. (Original) The system of Claim 2, further comprising a counter driven by a clock signal having a high-order bit driving said state line and lower-order bits driving respective ones of said timing lines.

4. (Original) The system of Claim 3, further comprising an address decoder receiving a multi-bit address signal and enabling in response thereto only one of said load lines.

5. (Original) The system of Claim 3, wherein count intervals of said counter are non-uniform in duration.

6. (Currently amended) A content addressable control section for controlling N time delays supplied to a plurality N of drive sections, comprising:

a multi-bit data bus;

N registers ~~seletively~~ selectively connected in parallel to said data bus;

~~at least one~~ control ~~line~~ lines connected to said N registers to reset said registers according to data on said data bus; and

~~a single~~ clocked ~~counter~~ counters connected to respective ones of said registers, started by a trigger signal, and providing ~~an output~~ outputs in ~~comparision~~ comparison to said connected registers.

7. (Original) The control section of Claim 6, wherein said trigger signal is synchronous with a clock signal.

8. (Original) The control section of Claim 6, wherein said trigger signal is aperiodic.

9. (Currently amended) The control section of Claim 6, wherein said registers and counters are arranged in rows and columns and wherein ~~seach~~ each of said registers is controlled by a row enable signal, a column enable signal, and a load signal.

10. (New) An actuator array and control system therefor, comprising:

a plurality of actuators;

a plurality of drivers driving respective ones of said actuators;

an overall controller outputting a multi-bit clock bus and a multi-bit data bus;

a plurality of control sections controlling respective ones of said drivers and each comprising:

a latchable register receiving said multi-bit data bus;

a decoder receiving said multi-bit clock bus and storing an address unique to each of said control sections and causing said register to latch data on said multi-bit data bus in

response to a comparison of said multi-bit clock bus and said unique address; and

an output latch controlling said respective one of said drivers in response to a comparison of said latched data and said multi-bit clock bus.

11. (New) The actuator array and control system therefor of claim 10, wherein said overall controller outputs to all of said control sections a first control signal to enable all of said decoders and a second control signal to enable all of said output latches.